Amendments to the Specification:

Please replace paragraph number **[0013]**, on page 2, with the following amended paragraph:

Fig. 14 is a table of simulation parameters and simulation results for the interconnect structure of Fig. 8A compared to current and voltage values for the standard interconnect structure of Fig. 1B~~Fig. 1~~.

Please replace paragraph number **[0016]**, on page 3, with the following amended paragraph:

Fig. 16 compares stress reduction of the standard interconnect structure of Fig. 1B with the structure of Fig. 8A, which has two thick metal layers~~ 212, 218~~.

Please replace paragraph number **[0018]**, on page 4, with the following amended paragraph:

Fig. 1B illustrates a conventional interconnect structure 100 ~~and bumps 112A, 112B~~ of Fig. 1A. The interconnect structure 100 (Fig. 1B) may be on the die 133 (Fig. 1A) as part of a backend interconnect of a microprocessor. The interconnect structure 100 in Figs. 1A and 1B may include~~ solder bumps 130,~~ a top metal layer 104, a passivation layer 106, a polyimide layer 108, a ball limited metallization (BLM) layer 110 and C4 bumps 112A-112B. "BLM" may also stand for base layer metallization.

There may be several metal layers under the top metal layer 104, and there may be transistors under the metal layers.

Please replace paragraph number **[0019]**, on page 4, with the following amended paragraph:

The C4 bumps 112A-112B in Figs. 1A and 1B may transfer current from the solder bumps 130 (Fig. 1A) to the top metal layer 104 (Fig. 1B). The top metal layer 104 may transfer current to the metal layers under the top metal layer 104, which transfer current to underlying transistors in the die 133~~die 102~~. It may be desirable to limit or reduce a maximum current (Imax) through a specific C4 bump, such as the C4 bump 112B, to the top metal layer 104 to increase bump reliability.

Please replace paragraph number **[0036]**, on page 9, with the following amended paragraph:

As shown in Fig. 1C, if a current driver (i.e., transistor) 160 demands a high current, current 162 has to come through one C4 bump 112A because the current 162 cannot be spread by more than~~spread more then~~ one bump pitch.

Please replace paragraph number **[0037]**, which begins on page 9, with the following amended paragraph:

Fig. 1D shows a simplified version of the thick metal interconnect structure 800 shown in Fig. 8A. In Fig. 1D, current 250 can be spread by more than~~spread more then~~ one bump pitch. Current 250 from the substrate 128 may be spread to multiple solder bumps 130A, 130B and then multiple C4 bumps 112A, 112B. The current 250 may then be spread through one or more thick metal layers 218 to the top metal layer 202, which is coupled to a high current demand driver 160. In this way, current 250 may come from multiple bumps 230A, 230B instead of one bump 112A (Fig. 1C), which can reduce current from one bump 230.

Please replace paragraph number **[0039]**, on page 10, with the following amended paragraph:

Fig. 14 (described below) lists examples of maximum current values through the bumps 230A-230D. A maximum current through each bump 230A, 230B in Figs. 8A and 8B may be lower than the maximum current through each bump 112A, 112B in Fig. 1B~~Fig. 1.~~ because the bumps 230A, 230B in Figs. 8A and 8B are coupled to thick metal layers 212, 218. The bumps 112A, 112B in Fig. 1B ~~Fig. 1~~ are not coupled to thick metal layers. Each bump 112 in Fig. 1B ~~Fig. 1~~ may have to carry a full desired current, such as 680 mA, to the top metal layer 104.

Please replace paragraph number **[0054]**, which begins on page 14, with the following amended paragraph:

Fig. 14 is a table of simulation parameters and simulation results for the interconnect structure 800 of Fig. 8A (with two thick metal layers 212, 218) compared to maximum current and voltage drop for the standard interconnect structure 100 of Fig. 1B~~Fig. 1~~. The standard interconnect structure 100 of Fig. 1, with no thick metal layers, is represented by row 1310 in Fig. 14. The standard interconnect structure 100 of Fig. 1 may have, for example, a maximum current (Imax) through the bump 112 of 680 mA, and a voltage drop (V = IR) from the bump 112 to the top metal layer 104 of 29 mV.